**Dr. R. JAYAGOWRI**

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**Web of Science id** ABW-7876-2022

## *Educational Qualifications:*

- **Ph.D (VLSI _DFT) (2008-2014)** in Jawaharlal Nehru Technological University, Hyderabad in the year 2014.
- **M. E (APPLIED ELECTRONICS) -** in College of Engineering, Guindy, Anna University, Chennai in the year 2004. **CGPA: 8.3 (First class with Distinction)**
- **B.E. (Electronics and communication Engineering)** from Bharathidasan University, Trichy in the year 1992. **(First class)**

## *Professional Experience:*

- **August 2014 onwards -** Associate professor (PG VLSI stream) in Department of ECE, BMS College of Engineering, Bangalore
- **July 2008 to August 2014 -** Associate Professor in the Dept of ECE, K.S.I.T, Bangalore
- **Apr 30, 2007 to May 1, 2008 -** Chief program Coordinator in RV-VLSI design center, Bangalore (Corporate trainer to Honeywell, NXP Semiconductors).
- **December 2006 to April 2007 –** faculty of engineering in ICFAI Tech, Bangalore.
- **June 2004 to July 2006 -** Senior Lecturer in the School of Electrical sciences, Vellore Institute of Technology, Vellore.
- **June 1998 to Aug 2002 -** Lecturer in Dept of ECE, Vellore Institute of Technology, Vellore
- **June 1993 to March 1996 -** Lecturer in Dept of ECE, Thanthai perriyar govt. institute of Technology, Vellore.

## *Patents*

- **Indian patent granted – Inventors:** *Ramamoorthy Jayagowri, Maithri Udaya Kumar Kenjoor Shetty* **Title:** "1pixel/1clock throughput modified median adaptive predictor for VESA DSC encoder" 20 years from the 3rd day of March 2020 in accordance with the provisions of the Patents Act,1970
  **patent number-347212**, **Application No: 202041009133** ***Date of Grant : 21/09/2020***
- **Indian patent granted - Inventors:** *Ramamoorthy Jayagowri, Shishira Shetty Kenjur Subhashchandra, Srijana Shankaranand Lali, BMS College of Engineering***Title:** "A Scan Architecture and a Method of Scan Based Testing to Reduce Shift Operations thereby Reducing Shift Power during Scan Testing" 20 years from the 23rd day of November 2021 in accordance with the provisions of the Patents Act,1970

**Patent No:400759, Application No: 202141053988.** ***Date of Grant : 04/07/2022***.

- **Indian patent filing** on "SIMULTANEOUS READ AND WRITE MEMORY CELL PRESERVING DATA INTEGRITY "in progress.
- **Indian patent filing** on "Automated Traditional Oil Lamp " in progress
- **Indian patent filing** on "A Method and System for Multiple Voice Disorder Detection " in progress.

### *Copyrights*

- Registered Copyright titled "IMPROVED TEMPOGRAM BASED IMAGE TEXTURAL DESCRIPTORS FOR VOICE DISORDER DETECTION" with Registration Number: L-136901/2023 on 29/11/2023 by Copyright office, Government of India. Applicant: BMSCE, Authors: ROOHUM JEGAN, R JAYAGOWRI
- Registered Copyright titled "ENHANCED GAMMATONE CEPSTRAL COEFFICIENTS FOR VOICE PATHOLOGY DETECTION USING DECISION TREE AND K-NEAREST NEIGHBOURS' CLASSIFICATION." with Registration Number: L-133046/2023 on 14/9/2023 by Copyright office, Government of India. Applicant: BMSCE, Authors: ROOHUM JEGAN, R JAYAGOWRI

### *Industry consultancy*

- Research consultancy - Involved in Developing a micro architecture for the MMAP prediction algorithm for VESA DSC 2.0 for a semiconductor industry Ignitarium solutions private limited, Bangalore(2019) for 0.5 Lakh

## ***Publications***

### Books Published

- Authors: R.Jayagowri, Pushpendra s Yadav : authored a book Titled "STATIC TIMING ANALYSIS FOR VLSI CIRCUITS" published by MEDTECH, A division of Scientific International Pvt. Ltd, New Delhi, ISBN: 978-93-87210-06-6, 1st edition in year 2018. *2nd Edition of the book Published on February 2024, ISBN :978-81-965445-6-0.*

- Authors: R.Jayagowri Titled "ANALOG & MIXED MODE VLSI DESIGN" as per VTU Syllabus for 6th Semester ECE Students, published by Sapna Book House, Bangalore, ISBN: 978-81-280-1121-4, 3rd edition in year 2015.

### Book Chapters:

- Book chapter titled " Windowed Modified Discrete Cosine Transform based Textural Descriptor approach for Voice Disorder Detection", book titled "Implementation of Smart Healthcare Systems using AI, IoT, and Blockchain", 1st Edition - September 27, 2022, eBook ISBN: 9780323919364, Paperback ISBN:9780323919166, DOI: https://doi.org/10.1016/B978-0-323-91916-6.00007-2 .Editors: Chinmay Chakraborty, Subhendukumar Pani, Mohd Abdul Ahad, Qin Xin, **Publisher: Elsevier**

## Technical Articles in Journals, Conferences and Edited Volumes

- Roohum Jegan, R.Jayagowri, “Enhancing Voice Disorder Detection Using Deep Transfer Learning Feature Fusion” 2024 IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation (IATMSI) Year: 2024 conducted by IIIT Gwalior.| Conference Paper | ***Publisher: IEEE (BEST PAPER AWARD RECEIVED) (web of science ESCI and Scopus indexed)***
- Roohum Jegan, R.Jayagowri ,"Voice pathology detection using optimized convolutional neural networks and explainable artificial intelligence-based analysis" in early access for publication in Computer Methods in Biomechanics and Biomedical Engineering, ***Taylor and Francis,*** 18th Oct 2023, 1-17 ***(web of science Q4).***
- Rohit praveen Mungekar, R.Jayagowri “Color tone determination prior algorithm for depth variant underwater images from AUV’s to improve processing time and image quality”, Multimedia tools and applications, ***Springer Nature***,28 February 2023, DOI: https://doi.org/10.1007/s11042-023-14773-*8* ***(web of science Q2 journal)***
- Kavya Bhat, R.Jayagowri "Descending Order Thermal Distribution Partitioning Algorithm for Flip-chip Packaged 3D ICs to Improve Heat Sinking and Reduce TSV Count" by authors, , in **IEEE Transactions on Components, Packaging and Manufacturing Technology,** Vol.10, Issue.7, Publication Year: 2020, Page(s):1148–1157,DOI:10.1109/TCPMT.2020.3003503, ***(web of science Q3 journal)*** https://ieeexplore.ieee.org/document/9120036,
- Bindushree V, R Jayagowri, “Implementation of Machine Learning in the Field of VLSI Placement: A Review”, An International Journal of Emerging Technologies and Innovative Research, , Volume 10, Issue 2, February 2023, pp 112-116, (ISSN-2349-5162) ***(UGC care Journal)***
- Roohum Jegan, R.Jayagowri, “MFCC and Texture Descriptors based Stuttering Dysfluencies Classification using Extreme Learning Machine”, ***International Journal of Advanced Computer Science and Applications (web of science indexed), Vol. 13, No. 8, 2022*** ISSN : 2156-5570 (Online), ISSN : 2158-107X (Print),, pp. 621-615. DOI: 10.14569/IJACSA.2022.0130870
- Roohum Jegan, R.Jayagowri, “An Evaluation of Various techniques of Voice disorder detection and Classification”, ***High Technology Letters, Volume 28, Issue 3, 2022*** ISSN NO : 1006-6748, pp. 198-207. https://doi.org/10.37896/HTL28.03/5413 ***(Active Scopus indexed)***

1. Sachin.K.Bhat, R.Jayagowri, “Gate Matching Algorithm for Early False Path Detection in Statistical Static Timing Analysis” proceedings of *IEEE international conference IEEE-SPICES 2022, published in IEEE Xplore digital library*. DOI: 10.1109/SPICES52834.2022.9774074 ***Publisher: IEEE (BEST PAPER PRESENTAR AWARD RECEIVED (web of science and Scopus indexed)***

- Mr. Rohit Pravin Mungekar, R. Jayagowri, “A Hardware Design of Red Channel Compensation Unit for Underwater Image Processing”, *Journal of Chengdu University of Technology (Science and Technology Edition)” Journal (Scopus Active Journal*), Volume 26, Issue 07, 2021, S.No.76, https://app.box.com/s/5qe2hqcecvtdiay7hao0a83scmf3dona ***Publisher: IEEE(web of science and Scopus indexed)***
- Neethu Johny, R.Jayagowri, “Standard Cell Optimization Techniques for Near Threshold Computing - A Review”, Presented in *IEEE 4th International Conference on Electronics, Communication and Aerospace Technology - ICECA 2020 on 5th November 2020*. The paper will be submitted for inclusion into *IEEE Xplore digital library*, **DOI:** 10.1109/ICECA49313.2020.9297602 ***Publisher: IEEE(web of science and Scopus indexed)***

- Neethu Johny, R.Jayagowri, "Performance and Variability Analysis on 7nm FINFET Circuits at near Threshold" presented in *2020, IEEE 2nd PhD Colloquium on Ethically Driven Innovation and Technology for Society, PhD EDITS 2020,* Access Number:9315308, **DOI:** 10.1109/PhDEDITS51180.2020.9315308 ***Publisher: IEEE(web of science and Scopus indexed)***
- Roohum Jegana , R.Jayagowri "Voice Disorder Detection And Classification- A Review", Second International Conference on IoT, Social, Mobile, Analytics & Cloud in Computational Vision & Bio-Engineering (ISMAC-CVB 2020), 29-30, October 2020*, (**ELSEVIER-SSRN**)* ISSN: 1556-5068,pp 253-267.
- Shishira Shetty K S, Dr R. Jayaygowri, "Enhanced FSS Architecture for Shift Power Optimization using Machine Learning", International Research Journal of Engineering and Technology (IRJET) Volume: 07 Issue: 11 | Nov 2020, Page 487-491, Impact Factor value: 7.529 |ISO 9001:2008 Certified Journal | e-ISSN: 2395-0056, p-ISSN: 2395-0072 https://www.irjet.net/archives/V7/i11/IRJET-V7I1179.pdf
- Abhinav Bijapur, Sumeet Siddappa Shirahatti, Dr. R. Jayagowri,"Power Optimization Techniques for NOC", International Journal of Engineering Research & Technology (IJERT),ISSN: 2278-0181.Vol. 9 Issue 07, July-2020. https://www.ijert.org/power-optimization-techniques-for-noc
- Kavya Bhat, R.Jayagowri, "Partitioning Technique for 3D ICs based on Power Density", in International Journal for Research in Applied Science & Engineering Technology (IJRASET) ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor: 7.177 Volume 7, Issue VII, July 2019. https://www.ijraset.com/fileserve.php?FID=24615
- Bhavana Adiga H P, R. Jayagowri "Application of Quantum Cellular Automata in Image Steganography with an Improved Fault Tolerant Majority Voter", 2018 *3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018), MAY 18th & 19th 2018.* https://ieeexplore.ieee.org/document/9012541. (**DOI:** 10.1109/RTEICT42901.2018.9012541). ***Publisher: IEEE(web of science and Scopus indexed)***
- Sujatha masillamani, R.Jayagowri "A review on Hybrid NOC", 2018 IEEE International Conference on Current trends towards Converging Technologies (ICCTCT 2018), March-2018. https://ieeexplore.ieee.org/document/8551009. DOI: 10.1109/ICCTCT.2018.8551009 ***Publisher: IEEE(web of science and Scopus indexed)***
- Shanthala .L , Jayagowri .R ; "Efficient Timing Closure in SOC through Timing Quality Checks and Engineering Change Order" published in International Journal of Advance Research, Ideas and Innovations in Technology, (Volume3, Issue3) May-2017, Page | 699-705, ISSN: 2454-132X. https://pdfs.semanticscholar.org/2082/fdbe491834242b4ca0b913f1a03f5179dff8.pdf

  Shanthala .L , Jayagowri .R ; "Simultaneous Data Path and Clock Path Engineering Change Order for Efficient Timing Closure in Complex SOC", published in IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) (*Scopus Indexed Journal*)Volume 7, Issue 3, Ver. I (May. - June. 2017), PP 35-41, e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197,DOI: 10.9790/4200-0703013541**.**

  http://www.iosrjournals.org/iosr-jvlsi/papers/vol7-issue3/Version-1/F0703013541.pdf
- Kiran JP, Dr. R Jayagowri, "Abstract, Correct by Construction and Faster Register Modeling of AMBA APB Bus", International Advanced Research Journal in Science, Engineering And Technology in Vol. 3, Issue 8, August 2016, pp 103-105, DOI 10.17148/IARJSET.2016.3818, ISSN (Online) 2393-802, ISSN (Print) 2394- 588. https://iarjset.com/upload/2016/august-16/IARJSET%2018.pdf

- R. Jayagowri **,** "Techniques for Low Power and Area Optimized VLSI Testing using Novel Scan Flip-Flop" published in International Journal of Computer Applications**(IJCA)** (0975 – 8887), Vol. 113 , No. 5, March 2015, pp 22- 28. ISBN : 973-93-80885-52-9**.**

  **https://pdfs.semanticscholar.org/fa98/f6241d3b98554bf376210e6b921ea615a2b6.pdf**

- R. Jayagowri and K. S. Gurumurthy, Gating Technique with Modified Scan Flip-flop for Low Power Testing of VLSI Chips, ***VLSI Design and Test Symposium (VDAT'12)***, July 2012, **Springer** LNCS 7373, pp(52-58). https://link.springer.com/chapter/10.1007/978-3-642-31494-0_7 ***(web of science and Scopus indexed)***

- Jayagowri, R., Gurumurthy, K.S : A Technique for Low Power Testing of VLSI Chips. In: Proceedings of IEEE International Conference on Devices, Circuits and Systems, IEEE DOI: 10.1109/ICDCSyst.2012.6188654, pp. 662 – 665, March 2012, pp.661-664. https://ieeexplore.ieee.org/document/6188654 , **DOI:** 10.1109/ICDCSyst.2012.6188654 ***Publisher: IEEE(web of science and Scopus indexed)***

- Vinay S, pramod K. P, R. Jayagowri, S. Ranjana & priyanka V, " Implementation of Low Power VLSI Architecture for Lossless Compressor and Decompressor", published in International Journal of Electronics and Communication Engineering(IJECE), ISSN(P): 2278-9901; ISSN(E): 2278-991X, Vol. 2, Issue 5, Nov 2013, pp 205-212.

- R. Jayagowri, karthik.S.Rao, Karthik.C.V, Keshava Koushik.S , "Design and Implementation of Low-Power Pipelined FFT Processor", Published in International Journal of VLSI & Signal Processing Applications, **ISSN 2231-3133**, Vol-2, Issue- 4,pp 330-335.

- R. Jayagowri and K. S. Gurumurthy, "Power Optimization during Shift Cycle of Scan based IC Testing ",published in the International Journal of Recent Trends in Engineering, by the Academy Publishers, Finland, **ISSN 2158-5555**, Vol.4, No.3, Nov 2010, pp 135-138.

- R. Jayagowri and K. S. Gurumurthy, "Design and Implementation of Area and Power Optimized Novel Scan flop", published in International journal of VLSI Design & Communication Systems (VLSICS), **ISSN 0976 – 1357**, Vol.2, No.1, March 2011, pp.37-43**.**

- Jayagowri, R., Gurumurthy, K.S : A Technique for Low Power Testing of VLSI Chips. In: Proceedings of **IEEE International Conference on Devices, Circuits and Systems**, **IEEE DOI: 10.1109/ICDCSyst.2012.6188654**, pp. 662 – 665, March 2012, pp.661-664. https://ieeexplore.ieee.org/document/6188654 , **DOI:** 10.1109/ICDCSyst.2012.6188654 ***Publisher: IEEE(web of science and Scopus indexed)***

- Jayagowri, R., Gurumurthy, K.S : A Review on testing of 3D ICs., In proceedings of International conference on VLSI & Signal processing (ICVSP-12),**ISBN 978-81-7286-723-2**,4-5 May2012, pp. 41-45.

- Jayagowri,R., Shivaprasad B, Srikanth K G : Design of an Efficient D Flip-Flop with Low Power Dissipation and Less Transistor Count, In proceedings of International conference on VLSI & Signal processing (ICVSP-12),**ISBN 978-81-7286-723-2**,4-5 May2012, pp. 18- 21.

- Shibani Nataraj, Vinay S, Jayagowri, R., A Proposed Clock Blocking Cell in Sequential Circuits, In proceedings of International conference on VLSI & Signal processing (ICVSP-12),**ISBN 978-81-7286-723-2**,4-5 May2012, pp. 22- 25.

- Jayagowri, R., Gurumurthy, K.S: An Area Optimised Combined Passtransistor and CMOS based method to implement Latch and Flip-Flop., In proceedings of International conference on Information Communication & Embedded Systems,24-25 February 2012organised by S. A.

Engineering college, in association with IEEE Chennai chapter, Technical Journals, Computer Society of India.

- Paper titled as "Power Optimization during Shift Cycle of Scan based IC Testing", is published in International Joint Journal Conference in Computer, Electronics and Electrical, CEE 2010conducted on 24-25 November-2010.
- Jayagowri, R., Gurumurthy, K.S: "Power and delay Optimized sequential circuit for VLSI Testing" International Conference on Communication Computation Control & Nanotechnology (ICN-2010) October 29 –30,2010 Organized by Departments of Telecommunication Engineering, Electronics & Communication Engineering and Instrumentation Technology, *R*ural Engineering College, Bhalki-585328.
- Jayagowri, R.: " Low power CMOS Technique implementation for real time image processing architecture", International conference on emerging microelectronics and interconnection technology, EMIT-08, conducted by **IMAPS India chapter** between December 15th to 18th,2008.
- Shruti K, R. Jayagowri, "VLSI Architecture of Colour Interpolation Processor for Real Time Video Application Using Adaptive Edge Enhancement Technique",NEWS-2016
- Jayagowri, R., Shibani Natraj, Shivaprasad:, "Reduction of power dissipation in a memory element", in national conference on Advances in Electronics and Intelligent computing-2011 on 2nd May 2011 conducted by East west Institute of Technology, Bangalore.
- Jayagowri, R., Gurumurthy K S ,"Power optimized high speed flip flop in the national conference on Networking , Embedded and wireless systems", (NEWS- 2010), conducted on 6th August – 2010, organized by Department of ECE, BMS College of engineering Bangalore.
- Jayagowri, R., Gurumurthy K S :" A Novel technique to implement the latch and FF", in the National conference on Recent advances in electronics and communication on 21st may 2010 organized by department of Electronics and Communication, New Horizon college of engineering, Bangalore.
- Jayagowri, R., Karthik: "power optimized combinational circuit', in the 4th National conference on advances in information technology, NCAIT – 2010,held on 8th may 2010, organised by Dept of Information science and engineering, SJB Institute of technology, Bangalore
- Jayagowri, R., Anitha:, "A novel VLSI architecture for image scaling in the 4th National conference on recent trends in communication electronics and information technology, NACTECIT 10, held on April 23-24. 2010 organised by CMRIT, Bangalore. Sponsored by ISRO, ministry of defence, ISTE, wiley publisher.
- Jayagowri, R., A. Abhishek, K. Chaitanya kumar: "power optimization in RTL Level" in the National conference on challenges in micro /Nano electronics conducted by IMAPS India Chapter and SIT, Tumkur on March 26-27, 2010.
- Jayagowri, R., C. Meena: " Power efficient technique for C & S unit in image processing Architecture", National conference on VLSI organised by TPGIT, vellore, Anna university on 12th August 2006.
- Jayagowri, R., Dr. N. Kumaravel: "Feature clustering and labeling for video object segmentation using ANN," National conference on emerging trends in engineering and technology, conducted by Dr. M.G.R educational and research institute, Deemed University, between May 1 – May3, 2004.

- Jayagowri, R.: “A view of telemedicine ECG, Blood pressure” in National Seminar electronics advances and trends conducted by Arunai engineering college between January 23 January 24, 2000
- Jayagowri, R., Dr. K. Chidambaram: “Optics a tool for biomedical engineering”, National Seminar on Bio-medical engineering. The Indian scenario 12th march – 13th march 1999. Organised b center for Bio medical engineering, Vellore Engineering College, between 12th & 13th March 1999.

## Awards & Recognition

- **Best paper award:** for the paper titled “Enhancing Voice Disorder Detection Using Deep Transfer Learning Feature Fusion” 2024 IEEE International Conference on Interdisciplinary Approaches in Technology and Management for Social Innovation (IATMSI) Year: 2024 conducted by IIIT Gwalior.| Conference Paper
- **Recognition:** Recognition of the IEEE 1st time journal Author-2020, Name of the Awarding Body/Agency IEEE Bangalore section awarded on 10/01/2021
- **Best paper award** for the paper titled “Implementation of power optimized High speed flipflop” in the national conference (NEWS 2010) conducted by BMS college of Engineering, Bangalore
- **Best paper award** for the paper titled “A Novel technique for implementation of latch and flip-flop” in the national conference conducted by New Horizon college of Engineering, Bangalore.
- **Best teacher award** for the year **OCT’ 98** in Vellore Engineering college (now Vellore Institute of Technology VIT University), Vellore.

## Awards along with Students work

- **PROJECT OF THE YEAR-KARNATAKA** :Titled “Hand Talk Using Flex Sensors with Voice Indication - Assistive Technology for the speech and Hearing Impaired” has won special seminar prize of “PROJECT OF THE YEAR-KARNATAKA” award 35th SERIES, SPP: 2011-12held on 13th and 14th July 2012 conducted by IISc, Bangalore.
- **Industry acknowledged award:** Titled “Low Power Pipelined FFT Processor Using self timed Adder” has won **WINNER AWARD** in the **All-India level Cadence Design Contest-2012** conducted by Cadence India Pvt Ltd, India. https://www.indiatechonline.com/it-happened-in-india.php?id=875
- **Industry acknowledged award** :Titled “Implementation of Low Power Pipelined VLSI Architecture for Mixed Bio Signal lossless Compressor using GRHF Coding Algorithm” was in the **Top-7** of the **Bachelor’s category –All India Level Cadence Design Contest 2013**
- UG student **project** Guided by me **won the first place** in the project exhibition conducted in K.S. Institute of Technology, Bangalore.

## Ph.D guidance Details

Supervising Ph.D, thesis entitled ;

- “Implementation and Characterization Approaches for Multiple Voice Disorder Detection Using Machine Learning and Soft Computing Techniques”.

- "Design And Characterize the Computational Elements for Sensor Node Processors at Near Threshold Region".
- "NOC for Wireless Network"
- "Built-In Self Repair Approach by Module Relocation for FPGA Based Reconfigurable Systems"

## Core Competency

- Ability to handle and solve design challenges in ASIC Design – Synthesis, DFT, Static Timing Analysis, Physical design
- Working knowledge of Linux, Vi editor, TCL, VHDL, Verilog.
- Working experience in EDA Tools

  Front end design: Design Compiler, Primetime, DFT Compiler, TetraMax (Synopsys tools), Xilinx, FPGA Advantage (MG tools), RTL compiler(cadence) Z-board and Basys3 board with Vivado

  Physical design: Astro (Synopsys tools), Microwind (Layout Editor), Encounter (cadence tool)

  Analog design: DesignArchitect (MG Tools), PSpice, Virtuoso(Cadence)

## Professional Activities:

## Important professional/editorial work:

- ***Organizer:*** TTTC VLSI Test workshop - the effort taken by Test technology Technical Council along with semiconductor industries to increase number of test engineers in India**.**
- ***Peer Reviewer***:

  (i) IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems-2024 and

  (ii) -IEEE Symposium on Circuits and Systems(ISCAS2022)-one of the flagship symposium
- ***Technical program committee member:*** *IEEE WINTECHCON-2023* Women in Technology conference on Emerging Technologies from silicon to software for a sustainable Future held on 21$^{st}$ September.2023 as well as committee member *IEEE WINTECHCON-2024*
- ***Tutorial co-chair:*** 7$^{TH}$ IEEE INTERNATIONAL TEST CONFERENCE INDIA 2021 (ITC INDIA-2023), held on JULY 25-27, 2023.
- ***Fellowship co-chair:*** 6$^{TH}$ IEEE INTERNATIONAL TEST CONFERENCE INDIA 2022 (ITC INDIA-2022).
- ***Session chair:*** session titled "Design for security and analog test" and fellowship co-chair for the 6$^{TH}$ IEEE INTERNATIONAL TEST CONFERENCE INDIA 2021 (ITC INDIA-2022), held on JULY 24-26, 2022 and session titled "Best Practices in Accelerated Pre-Silicon Verification, Analog & Stress Testing" for the 5$^{TH}$ IEEE INTERNATIONAL TEST CONFERENCE INDIA 2021 (ITC INDIA-2021), held on JULY 18-20, 2021.
- ***Board of study member:*** Academic Expert Member of Board of Studies-ECE in Sir M Visvesvaraya Institute of Technology, New Horizon college of engineering
- ***Reviewer and evaluator:*** 47th ALL India Students Design Competition- 2016 conducted by National Design and Research Forum (NDRF) and Institute of Engineers (IEI) during the month of September 2016.

## Technical courses:

- Successfully Completed NPTEL Online certification course on Machine Learning for Engineering and Science Applications conducted by IIT Chennai, from July-Oct,2019.

- Attended and completed the 2-week ISTE STTP workshop on CMOS Mixed-Signal and Radio Frequency VLSI Design, 30th January to 4th February 2017, Indian Institute of Technology Kharagpur NMEICT, T210KT-2017 with the Grade as Very good.

## Invited lectures given

- "Test Power Reduction for Recent IC Technology" for one week Faculty Development Program on Emerging Trends in Electronics, Communication and Networking Technologies 2022 conducted by Sree Vidyanikethan Engineering College (Autonomous), Tirupati, Andhrapradesh.
- TEQIP-II sponsored Finishing school courses on VLSI Physical Design conducted in COE, BMS college of Engineering from 1st August to 6th August 2016.
- "Low Power Issues on ASIC Design Flow" - Faculty Development programme on VLSI Design and Methodology at our college on 10th and 11th March 2016 at APS college of Engineering, Bangalore.
- Session on Introduction to CADENCE tools for Digital and Analog VLSI- Handson in the Faculty Development program on VLSI DESIGN USING CADENCE TOOLS conducted by K S Institute of Technology, Bangalore on June29-July03, 2015.
- National level workshop on Matlab Tools & Applications (MATAPP-2013) conducted by K.S. Institute of Technology, Bangalore.
- AICTE two-week refresher course on "Embedded systems and VLSI" during 19 June 2006 to 1 July 2006 on the topic combinational and sequential circuits using VHDL, pertaining to VLSI design on 28 June 2006.
- Titled as "ASIC Frontend Design" on 19/9/2005 in the Ganandipathy Tulsi Engineering College, Vellore.

## Technical lectures/Seminars/Workshops organised

- Organized and acted as a coordinator for *IEEE-TTTC VLSI Test Seminar Bangalore-2019* Bangalore by the IEEE Section Bangalore, on 21st & 22nd September-2019.
- **Coordinator and resource person** - TEQIP-II sponsored Finishing school course on VLSI Physical Design, BMS college of Engineering from 1st August to 6th August 2016.
- **Faculty coordinator** SMART COLLEGE SPHERE-Neighborhood Innovation Eco-Systems in conducted by BMS College of Engineering BMSCE IEEE on 12 March, 2016
- **Editor & Coordinator** - International Conference on Advanced trends in VLSI and Signal Processing (ICAVSP-2014) organized by Dept of ECE, K.S.Institute of Technology, Bangalore, 13-14 August, 2014.
- **Editor & Coordinator** - International Conference on VLSI and Signal Processing (ICVSP-2012) organized by Dept of ECE, K.S.Institute of Technology, Bangalore, 4-5 May, 2012.

- **Coordinator and resource person** - An intensive workshop on Image processing Technovision 04, organized by Dept of ECE, Vellore Institute of Technology, Vellore from oct'8-9Oct'9,2004
- A Short-term course on Basic VLSI Design, during November 30 – December 11, 2004.
- An extension series lecture on "Static timing analysis basic concepts – industry perspective"

## Technical lectures/Seminars/Workshops attended

- 5-Days National Level Online Faculty Development Program on "Machine Learning Approaches for Engineering Applications" from 27th Dec 2022 to 31st Dec 2022 (2.00pm-7.00p.m), organized by department of Information Information Technology, PRATHYUSHA ENGINEERING COLLEGE, Poonamallee- Thirivallur High Road, Thiruvallur-602025, Tamilnadu, India
- One Week National Level Online FDP on Societal Applications of Machine Learning, 26-30 December 2022 (9.00a.m to 1.30p.m) organized by the department of CSE at Shri Vishnu Engineering College for Women (A), Bhimavaram. He/She has cleared the end exam successfully.
- Two-Week Online Faculty Development Programme on "Applied Data Science" organized by the Department of Electronics and Communication Engineering in association with the Institution of Electronics and Telecommunication Engineers (IETE), Bangalore Centre conducted from 6th to 17th July 2020.
- Attended International Test Conference (ITC India-2019) by IEEE Bangalore chapter and ITC USA, in Bangalore on July 21-23, 2019.
- Attended the Capacity enhancement program on "FOCUS on Patents" conducted by BMS college of Engineering, in association with National Law school of Tndia University, Bangalore on 2nd March,2017 at BMS college of Engineering**.**
- Attended and completed the 2-week ISTE STTP workshop on CMOS Mixed-Signal and Radio Frequency VLSI Design, 30th January to 4th February 2017, Indian Institute of Technology Kharagpur NMEICT, T210KT-2017 with the Grade as Very good.
- Attended Cadence University conference on "Architecture to silicon systems: Academia's role in Electronic Design and R&D", held on December06, 2016, Bangalore.
- Attended the TEQIP-II Initiative 1 week Workshop on Modeling and Simulation of Thin Film Devices, conducted during 11th July -16th July, 2016, conducted by RV College of Engineering, Bangalore.
- Attended the Faculty Development program on IESA- Thought Leadership Forum on "Making chip test available for everyone" conducted by India Electronics and Semiconductor Association on June 29, 2016.
- Attended the training on Library characterization using Cadence Liberate tool on 30th -31st March, 2016 conducted by Cadence India Private Limited, Bangalore.
- Attended two days Training Program On Intellectual Property Rights on 4th February 2016 Organized by Department of Electronics & Communication Engineering BMS College Of Engineering, Bangalore In association with National Law School of India University, Bangalore
- Attended the All India conference on "MAKE in INDIA" Conducted by BVB College of engineering. Hubli-January 3rd-4th, 2016.

- Attended the 26th VLSI Design and 13th Embedded systems conference conducted by VLSI society of India, at Leela Palace, Bangalore on January 5-7, 2015.
- Attended a Faculty development workshop on system on chip design organized by ARM and Xilinx University Programme in Goa on December 16, 2014.
- A Seminar on Analog & Mixed signal conducted by mentor graphics higher education program on Mar – 11- 2010
- Two days VLSI Lab workshop conducted by DSCE in association with Cadence Design Systems ( I), Bangalore – 20th August 2009 to 21st August 2009
- Bridge course on Digital signal processing conducted by SANDS instrumentation PVT. LTD from 25th Feb 2002 to 11th March 2002.
- National Conference and workshops on technology today in cardiac and Neuro sciences conducted by center for medical electronics, college of engineering, Guindy, Anna university, Chennai between may 26th to 27th , 2000.

## Academic Administration:

- ***Convener:*** College Internal compliance committee of BMSCE to support the human rights in workplace. (2022-2025)
- ***Research committee member:*** Department Research committee member(ECE) 2024
- ***Advisory Board member:*** Department DAB member(ECE) 2022-24
- ***Editor& Convener:*** Department Magazine committee (ECE) 2022.
- ***Department Academic committee member:*** Department DAC member(ECE) 2020-23
- ***Board of study member:*** Academic Expert Member of Board of Studies-ECE in Sir M Visvesvaraya Institute of Technology (2024-2026), New Horizon college of engineering (2023-2025)
- ***Internship coordinator***: Coordinator for M.Tech (VLSI &ES) from 2015 to till now.
- ***Project coordinator***: Coordinator for M.Tech (VLSI &ES) from 2015 2023.
- ***Editor & Coordinator***: International Conference on Advanced trends in VLSI and Signal Processing (ICAVSP-2014) August, 2014 & 2013).
- ***Program coordinator***: corporate training for NXP semiconductor in RV VLSI design center (2006-07).
- ***Program coordinator***: M.tech VLSI design coordinator and incharge in VIT, Vellore (2004-06).