INDIVIDUAL FACULTY PROFILE- TEMPLATE TO BE UPLOADED IN COLLEGE WEBSITE

Name in Caps : PRIYADARSHINI JAINAPUR
Designation : Assistant Professor
Qualification : B.E, M.Tech.
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Experience Total : 09 years
Teaching experience : 09 years
Date of Joining this Institution (BMSCE): 12/06/2023

Research Interests:

VLSI Design and Embedded Systems, Verilog HDL, Mixed Signal Design, Real Time Systems.

About Your self	I have about **09 Years of total Experience**. Specialized in VLSI Design , I had worked as a Assistant Professor in BMS Evening College of Engineering, Bangalore for 09 years. I would like to serve the student community being a good facilitator.
Education:	**Masters:** **M.Tech** (VLSI Design and Embedded System) VTU, Belgaum, Karnataka **Bachelors:** B.E. (Telecommunication Engineering) From BMSIT V.T.U., Belgaum, Karnataka
Journals Published	1. "Modeling and Design of a CMOS Low Drop-out (LDO) Voltage Regulator" - International Journal of VLSI and Embedded Systems-IJVES (ISSN: 2249 – 6556) 20-June-2013 2. " A model for automated detection and control of air pollution from vehicles" -Int. J. Engg. Sc. & Mgmt. Vol. VII | Issue II | Jul - Dec 2016 3. " A model for Face recognition system using voila-jones Algorithm," - Int. J. Engg. Sc. & Mgmt. Vol. VII | Issue II | Jul - Dec 2017
Conferences / workshops attended	1. Participated in ISTE- BMSCE Chapter one week faculty development programme on "Outcome Based Education" between 16 /8/2022 to 20/08/2022 organized by B.M.S. Evening college of Engineering. 2. Participated and Successfully completed One Week AICTE – VTU Joint Teachers Training Programme on "An Overview of Teaching Techniques in Data Science and Analytics" between 25th & 29th April 2022 Organized by VTU Human Resource Development Centre (VTU - HRDC), Centre for PG Studies, VIAT. 3. Participated and Successfully completed One Week Teacher Traning Programme AICTE – VTU on "Introduction to Python Programming & its Applications" 13th -17th March 2023. 4. Participated and Successfully completed One Week Teacher Traning Programme AICTE – VTU on "Analog VLSI Design using EDA Tools" 20th -25th March 2023. 5. Participated and Successfully completed One Week programme on "Research Methodology - Tools and Techniques' 5th Sept – 9th Sept 2022 6.

Courses Handled	Fundamental of VLSI, VLSI Design, Verilog HDL, Operating Systems, Computer Communication Networks, Embedded Systems. Real Time Operating Systems.
Additional Responsibilities	1.Department Co-Ordinator for Dept of ECE, BMSECE from 2016- till Date 2. Member of BMSECE Women Cell. 3.